PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-211128
(43)Date of publication of application : 20.08.1993

(51)Int.Cl. H01L 21/205
H01L 21/265
H01L 21/027
H01L 27/12
H01L 31/04

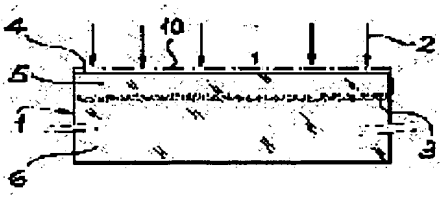
(21)Application number : 04-246594
(22)Date of filing : 16.09.1992

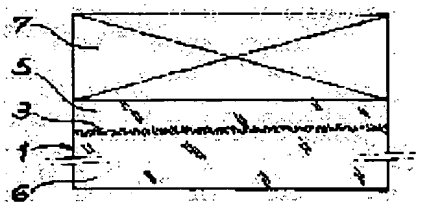
(71)Applicant : COMMISS ENERG ATOM
(72)Inventor : BRUEL MICHEL

(30)Priority
Priority number : 91 9111491 Priority date : 18.09.1991 Priority country : FR

(54) MANUFACTURE OF THIN SEMICONDUCTOR FILM

(57)Abstract:
PURPOSE: To manufacture a uniform quality and thin semiconductor film by maintaining a wafer temperature during hydrogen or rare-gas ion implantation which is lower than a gas discharge temperature and performing heat processing, while a wafer and a reinforcing material are in close contact with each other.
CONSTITUTION: A fine bubble layer 3, which defines a semiconductor wafer 1 as a low region 6 and an upper region 5 constituting a thin film, is caused by implantation to a surface 4 of the wafer 1 by a bombardment 2. Ions are selected from hydrogen gas or rare-gas ions. The wafer temperature during the implantation is maintained to be lower than a temperature for discharging the ion gas from the semiconductor. The flat surface 4 of the wafer 1 is brought into close contact with a reinforcing material 7 of a rigid material layer. By performing heat processing at a temperature of 500° C or higher which is appropriate to separation of the thin film 5 from the bulk of the substrate 6 by a crystal rearrangement in the wafer 1 and pressure in the fine bubbles, and selecting the implantation energy, the thickness of the thin film can be selected within a wide thickness range.





LEGAL STATUS

[Date of request for examination]	28.11.1995
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3048201
[Date of registration]	24.03.2000
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

1. JP,3048201,B

* NOTICES *

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CLAIMS

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(57) [Claim(s)]
[Claim 1] When it is the manufacture approach of a semiconductor material thin film, a semiconductor material is substantially [the field of a semiconductor material wafer / as the main crystal faces] parallel completely in the case of the quality of a single crystal and a semiconductor material is polycrystal The semiconductor material wafer with which the field of a semiconductor material wafer inclines slightly to the main crystal faces of the same characteristic to all the particles of a polycrystal ingredient The following three phases : the layer of the minute air bubbles which demarcate the lower part area which constitutes the mass of a substrate, and the upper part area which constitutes a thin film in the volume of said wafer Make it generated in the volume of said wafer of the depth near the average penetration depth of ion. It is the 1st step of the ion implantation to the field of said wafer, and ion is chosen from hydrogen gas ion or rare gas ion. The wafer temperature under impregnation The 1st step where the gas generated by impregnation ion is maintained lower than the temperature which may be emitted from a semi-conductor by diffusion, While it was higher than the stiffener which consists of at least one rigid ingredient layer, the 2nd step to which it is made to stick, and the temperature at which an ion implantation is carried out and said stiffener and flat surface of said wafer had stuck the flat surface of said wafer all over this phase The approach of the thin film characterized by including processing in the 3rd step which heat-treats the assembly of said wafer and said stiffener at the temperature suitable for making a thin film and the mass of a substrate separate according to a rearrangement operation of the crystal in a wafer, and the pressure operation in minute air bubbles.
[Claim 2] The manufacture approach of the thin film according to claim 1 characterized by carrying out the impregnation phase of the ion into a semiconductor material through one or more ingredient layers of the property which can cross ion, and thickness.
[Claim 3] The manufacture approach of the thin film according to claim 1 characterized by a semi-conductor having IV group's covalent bond.
[Claim 4] The manufacture approach of a thin film given in any 1 term of claims 1-3 which a semi-conductor is silicon, impregnation ion is hydrogen gas ion, and the wafer temperature under impregnation is 20-450 degrees C, and are characterized by the temperature of the 3rd heat treatment phase exceeding 500 degrees C.
[Claim 5] The manufacture approach of the thin film according to claim 2 characterized by being the silicon wafer with which impregnation was carried out through the enclosure high-temperature-oxidation silicon layer and, by which the stiffener was covered in at least one silicon oxide layer.
[Claim 6] The manufacture approach of the thin film according to claim 1 characterized by carrying out the 2nd step to which the flat surface of said wafer is stuck with a stiffener by applying electrostatic stress.
[Claim 7] The manufacture approach of the thin film according to claim 1 characterized by adhering by one or more approaches chosen from the groups which a stiffener becomes from the chemical vacuum deposition which is not supported with the chemical vacuum deposition, plasma, or photon supported with vacuum evaporationo, the plasma, or a photon.
[Claim 8] The manufacture approach of the thin film according to claim 1 characterized by combining a stiffener with said wafer with the adhesive matter.
[Claim 9] The manufacture approach of the thin film according to claim 1 characterized by being made to adhere to a wafer by the processing whose stiffener promotes an interatomic bond.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to a thin semiconductor material film (semiconductor material thin film) and the desirable manufacture approach applicable to manufacture of the nature film of a single crystal.
[0002]
[Description of the Prior Art] Although there are various approaches in manufacture of the nature semi-conductor film of a single crystal, while manufacture of a polycrystal ingredient film or an amorphous ingredient film is comparatively easy, since it is far difficult, operation of these approaches often has complicated manufacture of the nature film of a single crystal, and it is known that costs will start.
[0003] The approach currently used for manufacture of the so-called "silicon-on-insulator" substrate is in the approach currently used for manufacture of the nature film of a single crystal. The purpose of this approach is manufacturing the nature silicon film of a single crystal located on the substrate electrically insulated from the film.
[0004] By the crystal growth hetero epitaxy method, a lattice parameter can grow up the silicon crystal of a thin film on the nature substrate of a single crystal of other molds near the parameter of silicon, for example, silicon on sapphire, (aluminum 2O3), and a calcium-fluoride substrate (CaF2). . (see the bibliography 5).
[0005] In order to prepare the silicon oxide layer which separates the nature silicon film of a single crystal from the mass of a substrate in silicon volume circles, impregnation of ion with much oxygen dosage into a silicon substrate is being used for the SIMOX method (this name is used by reference). (Bibliography 1 reference) .
[0006] The principle of chemical or flake-izing (thinning) of the wafer by mechanochemical wear is being used for other approaches. The approach which stored a success most by this category is using the principle of a dirty stop further. By this approach, shortly after required thickness is reached, flake-ization of a wafer can be stopped, and it can do in this way, and uniform thickness can be secured. This approach performs p mold doping to n mold substrate covering the whole thickness of the film with which it asks for manufacture, and subsequently, it is activity and becomes n mold silicon from carrying out chemical etching of the substrate to p-type silicon by the inactive chemistry bath (see the bibliographies 2 and 3).
[0007] The main applications of the nature semi-conductor film of a single crystal are the insulator top silicon substrate for manufacture of the integrated circuit which has an X-ray-lithography mask, a sensor, a solar battery, and two or more barrier layers, the independence silicon film, or the independence carbonization silicon film.
[0008] The thin various manufacture approaches of the nature film of a single crystal have a fault about a manufacture procedure.
[0009] The hetero epitaxy method is restricted by the class of substrate. Since the lattice parameter of a substrate is not the same to the parameter and precision of a semi-conductor, a film has a defect on much crystals. Furthermore, these substrates are expensive, and are weak, and exist only with the limited dimension.
[0010] The SIMOX method needs an ion implantation with very much dosage, and this impregnation requires a very heavy and complicated impregnation machine. Probably, it will be difficult to restrict the output of such a machine and to increase an output remarkably.
[0011] A flake-ized method is not competitive from a viewpoint of homogeneity and quality except for the case where the principle of a dirty stop is used. An approach becomes complicated by installation of this dirty stop, and use of a film may be restricted to an unfortunate thing depending on the case.
[0012] Therefore, if a dirty stop is carried out by p mold doping to n mold substrate, the electron device of the arbitration manufactured within a film is fitted to p mold property of a film, and if it is ****, there will be. [no]
[0013]

[Problem(s) to be Solved by the Invention] It is related with the manufacture approach of the thin semiconductor material film which enables manufacture of the film which has the thickness which this invention could conquer the fault which mentioned above the initial substrate with which the class differed from the semi-conductor chosen, and very many impregnation dosage, without also needing a dirty stop, and was still more homogeneous, and was adjusted.
[0014]
[Means for Solving the Problem] When the manufacture approach of this thin film has a substantially [the field of a semiconductor material wafer / as the main crystal faces] parallel completely semiconductor material in the case of the quality of a single crystal and a semiconductor material is polycrystal The semiconductor material wafer with which the field of a semiconductor material wafer inclines slightly to the main crystal faces of the same characteristic to all the particles of a polycrystal ingredient The following three phases : the layer 3 of the minute air bubbles which demarcate the lower part area 6 which constitutes the mass of a substrate, and the upper part area 5 which constitutes a thin film in the volume of said wafer Make it generated in the volume of said wafer of the depth near the average penetration depth of ion. It is the 1st step of the ion implantation to the field 4 of said wafer 1, and ion is chosen from hydrogen gas ion or rare gas ion. The wafer temperature under impregnation The 1st step where the gas generated by impregnation ion is maintained lower than the temperature which may be emitted from a semi-conductor by diffusion, While it was higher than the stiffener 7 which consists of at least one rigid ingredient layer, the 2nd step to which it is made to stick, and the temperature at which an ion implantation is carried out and said stiffener and flat surface of said wafer had stuck the flat surface 4 of said wafer all over this phase It is characterized by including processing in the 3rd step which heat-treats the assembly of said wafer 1 and said stiffener 7 at the temperature suitable for making a thin film 5 and the mass of a substrate 6 separate according to a rearrangement operation of the crystal in a wafer 1, and the pressure operation in minute air bubbles.
[0015] therefore, this invention has the parallel main crystal faces (this side -- all semi-conductor particles -- receiving -- the same characteristic -- for example, (1, 0, 0), it has) in a semi-conductor side substantially [all the particles that constitute a grid] -- if it becomes, it will be applied also to a polycrystal semiconductor material. ZMRSOI (ZMR= band-melting-recrystallization) may be mentioned about a semiconductor material (see the bibliography 4). Vocabulary called an impregnation phase means 1 time of an impregnation phase, and continuation of impregnation with different dosage, different energy, and/or different ion.
[0016] It is advantageous to carry out the ion implantation into a semiconductor material through one or more ingredient layers as a modification of this invention approach, and it obtains. Ion penetrates this ingredient layer, and a ** "enclosure (encapsulating)" layer is chosen so that it may advance into a semi-conductor. For example, an enclosure layer may be used also as a means to adjust the physicochemical condition of a semi-conductor side also as a means to protect a semi-conductor from the contamination which may be considered also as a means to suppress penetration of the ion into a semi-conductor, in order to manufacture the thinner film. When the substrate which constitutes a wafer is manufactured from silicon, it is advantageous to consist of high-temperature-oxidation silicon, and to choose the enclosure layer whose thickness is 25-500nm, and it obtains. or [that these enclosure layers may be held after an impregnation phase] -- or it may be removed.
[0017] In this invention, it is maintained lower than the critical temperature which the gas generated by impregnation ion diffuses temperature quickly as a result by always adjusting during an activity the temperature of the wafer with which an ion implantation is carried out, and is emitted from a semi-conductor. For example, in the case of hydrogen impregnation to silicon, this critical temperature is about 500 degrees C. If this temperature is exceeded, since minute air bubbles will not be formed, the effectiveness of this approach is lost. In the case of silicon, the impregnation temperature of 20-450 degrees C is desirable.
[0018] All over 3rd step called heat treatment of a wafer stiffener assembly, the rearrangement of a crystal arises following the non-order generated by the ion implantation. A film and a substrate are separated by the rearrangement of the crystal both produced by the 3rd-step heat treatment, and condensation of the air bubbles which produce macroscopic air bubbles. Under an operation of the gas pressure force in these air bubbles, a semi-conductor side receives high stress. If to avoid generation of the blister condition equivalent to the macro air bubbles formed [which were formed and were front-face-transformed] is wished, it is important to compensate such stress. Therefore, before macroscopic air bubbles reach the last growth step and condense a blister condition mutually, it can become in pieces small. Therefore, if it asks for manufacture of a continuous semi-conductor film, it is required to compensate the stress produced all over a heat treatment phase. If based on this invention, this compensation will be performed by sticking a semiconductor wafer side and a stiffener. The function of a stiffener is that the stress generated by macroscopic air bubbles is compensated by contact and its mechanical characteristic with a wafer side. Therefore, a semi-conductor film may not always be spoiled [flat and] among a heat treatment phase until it finally ****.

[0019] If based on this invention, selection of the manufacture approach of a stiffener and the class of stiffener will be decided by each application a film is considered to be. For example, if the application meant is manufacture of an insulator top silicon substrate, as for a stiffener, it will be advantageous to consist of a silicon wafer covered with at least one dielectric layer like an oxide layer or a nitride layer, and it will be obtained. The oxide of a stiffener is stuck from it with the wafer with which a film should be manufactured, and the wafer has for example, the silicon oxide enclosure layer in arbitration.
[0020] A several micrometers - dozens of micrometers stiffener may be manufactured on a wafer by approach like the chemical vacuum deposition which is not supported with the chemical vacuum deposition, plasma, or photon supported with evaporation, the plasma, or a photon, if the thickness which might be combined with the wafer or was chosen about the stiffener is suitable (i.e., if it becomes).
[0021] Vocabulary called adhesion means the contact acquired by pressing a stiffener on a wafer by electrostatic stress and/or adhesion contact.
[0022] Therefore, the stiffener of this invention may be combined with a semiconductor wafer by manufacturing previously at least one of the front faces which should be combined, and carrying out heat treatment and/or the electrostatic processing accompanied by selection of a pressure to arbitration, in order to help the interatomic bond of a stiffener and a semiconductor wafer, when the adhesive matter is used for both a stiffener and a wafer or it does not ask for use of the adhesive matter further. A wafer may adhere to a stiffener also by electrostatic stress.
[0023] About the application about manufacture of self-supported film, it is appropriate to choose the class of stiffener so that a stiffener can be separated from a film simply and alternatively. By reference, in order to manufacture the nature silicon film of a single crystal, it is possible to choose a silicon oxide stiffener and this stiffener is removed from it in a hydrofluoric-acid bath after the 3rd heat treatment phase of a process.
[0024] As a description of this invention approach, selection of the working temperature in the 2nd step and the 3rd step must suit the following requirements. In order to install a stiffener on a wafer, don't apply the temperature which may make the 3rd-step processing start. For this reason, if based on this invention, it is required at temperature lower than the temperature of the 3rd-step heat treatment to carry out the 2nd step of a process. By this invention, this heat treatment must be carried out at the temperature which a crystal rearrangement and condensation of air bubbles produce effectively. For example, the temperature which exceeds about 500 degrees C for a crystal rearrangement and condensation of air bubbles to arise in suitable dynamics in the case of silicon is required.
[0025] In enforcing this invention approach, the ion used for impregnation by bombardment is usually H+ ion, but it should not be considered that this selection is restrictive. Therefore, it is used for it for the ion of rare gas like a molecule hydrogen ion or helium, neon, a krypton, and a xenon, the principle of this approach being independent or combining, and may be applied. In order to apply this invention approach industrially, IV group semi-conductor is desirable, for example, use of a silicon, germanium, carbonization silicon, and silicon-germanium alloy is possible.
[0026]
[Example] With reference to an accompanying drawing, the nonrestrictive example of this invention is further explained to a detail.
[0027] The example to be explained with reference to an accompanying drawing from now on is related with manufacture of the thin film within the nature silicon wafer of a single crystal by H+ ion implantation.
[0028] If H+ ion (proton) is poured into the nature silicon wafer of a single crystal with which the front face is equivalent to the main crystal face, for example, (1, 0, 0), a field, by 150keV(s), when there is little impregnation dosage (<1016cm-2), the hydrogen concentration profile C to depth P which has the maximum concentration in the depth Rp as shown in drawing 1 will be obtained. In proton impregnation into silicon, Rp is about 1.25 micrometers.
[0029] In the dosage of abbreviation 1016cm-2, an impregnation hydrogen atom begins to form air bubbles, and these air bubbles are distributed near the field parallel to a front face. The surface field is the same also about the minute air-bubbles side which is equivalent to the main crystal faces, and turns into ****** as a result.
[0030] It is possible to make fusion of the air bubbles made to **** silicon in the impregnation dosage exceeding 1016cm-2 (for example, 5.1016cm-2) into two parts of the upper part film (thin film) whose thickness is 1.2 micrometers, and the mass of a substrate start with heating.
[0031] Hydrogen impregnation is an advantageous example. It is because the braking process of the ion in the inside of silicon is ionization (electronic braking) as a matter of fact. Nuclear mold braking by atomic migration is produced only at the last of range. So, in the surface layer of silicon, air bubbles are focusing near the depth Rp (depth of the maximum concentration) covering the thickness which produced only very few defects and was limited. For this reason, the effectiveness of this approach required for appropriate impregnation dosage (5.1016cm-2) is attained, and after separating a surface layer, it becomes possible to obtain the front face where roughness was limited.

[0032] If this invention approach is used, it will become possible by choosing impregnation energy to choose the thickness of a thin film by large thickness within the limits. This property is much more important, because the atomic number z of impregnation ion is small. For example, the following tables show the thickness of the film which may be obtained to the impregnation energy from which H+ ion (z= 1) differs.
Energy [of H+ ion] (keV) 4.7 13.5 drawing 2 showed the semiconductor wafer 1 covered with the enclosure layer 10 by arbitration, and this layer has received the ion bombardment 2 of H+ ion which lets the flat surface 4 parallel to the main crystal faces pass. 10 50 100 150 200 500 Thickness of 1000 films (micrometer) 0.1 0.5 0.9 1.2 1.6 The minute air-bubbles layer 3 can be accepted in parallel with a field 4. The layer 3 and the field 4 limit the thin film 5. Other parts of the semi-conductor substrate 6 constitute the mass of a substrate.
[0033] Drawing 3 shows the field 4 of a semiconductor wafer 1, and the stiffener 7 to which it was stuck. In the advantageous example of this invention, the ion implantation to an ingredient is performed through the high-temperature-oxidation silicon enclosure layer 10, and the stiffener 7 consists of a silicon wafer covered with at least one dielectric layer.
[0034] Since a stiffener is fixed to a semiconductor material, electrostatic stress is being used for other examples. The silicon stiffener which has the silicon oxide layer of 5000A thickness in this case is chosen. The flat surface of a wafer is contacted to the oxide of a stiffener, and the dozens of volts potential difference is applied between a wafer and a stiffener. The pressure obtained here is several 105-106 pascals.
[0035] Drawing 4 shows the film 5 which was isolated by space 8 from the mass of a substrate 6 and which was combined with the stiffener 7.
[0036] Refer to the following data for this specification.
(1)SIMOX SOI for Integrated CircuitFabrication by Hon Wai Lam, IEEE Circuits and Devices Magazine, July 1987.
(2)Silicon on Insulator Wafer Bonding, Wafer Thinning, Technological Evaluations by Haisma, Spierings, Biermann et Pals, Japanese Journal of Applied Physics, vol.28,no.8,August 1989.
(3)Bonding of silicon wafers for silicon on insulator by Maszara,Goetz,Caviglia and McKitterick, Journal ofApplied Physic 64(10)15 November 1988.
(4)Zone melting recrystallization silicon on insulator technology by BorYeu Tsaur, IEEE Circuits and Devices Magazine, July 1987.
(5)1986 IEEE SOS/SOI Technology Workshop, September 30-October 2, 1986,South Seas plantation resort and yacht Harbour, Captiva Island, Florida.

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DRAWINGS

[Drawing 1]

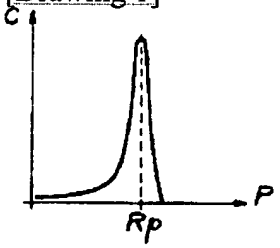

FIG. 1

[Drawing 2]

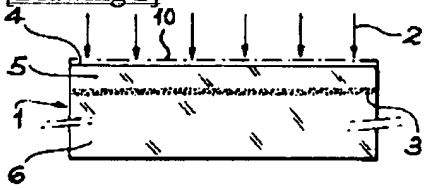

FIG. 2

[Drawing 3]

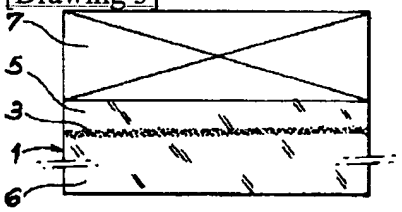

FIG. 3

[Drawing 4]

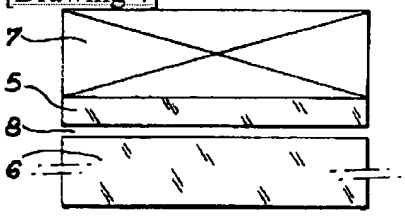

FIG. 4

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